#### COMP 122/L Lecture 12

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Slides adapted from Dr. Kyle Dewey

#### Outline

- Memory instructions
  - Load (ldr)
  - Store (str)
- Arrays

# Memory Operations

#### Refresher

You've already seen one form of 1dr for handling strings

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```
.data
my_string:
    .asciz "hello"

.text
ldr r0, =my_string
```

#### Refresher

You've already seen one form of ldr for handling strings

```
.data
my_string:
    .asciz "hello"
```

.text
ldr r0, =my\_string

Puts starting address of "hello" in r0

<sup>-</sup>This was used for setting up swi instructions

<sup>-</sup>While this uses memory, it did so indirectly (the swi instruction actually read the memory, not us)

## Putting Integers in Memory

.word directive will put a 32-bit integer in memory, much like .asciz will put a string in memory

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.word directive will put a 32-bit integer in memory, much like .asciz will put a string in memory

```
.data
my_string:
    .asciz "hello"
first_int:
    .word 42
second_int:
    .word 38
```

Step I: use ldr to put its address into a register...

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```
.data
first_int:
   .word 42
second_int:
   .word 38

.text
ldr r0, =first_int
```

Step 2: use ldr with [] to read the value at the address

```
.data
first_int:
   .word 42
second_int:
   .word 38

.text
ldr r0, =first_int
```

Step 2:use ldr with [] to read the value at the address

```
.data
first int:
  .word 42
second int:
  .word 38
  .text
ldr r0, =first int
ldr r1, [r0]
```

Step 2:use ldr with [] to read the value at the address

```
.data
first_int:
   .word 42
second_int:
   .word 38

.text
ldr r0, =first_int
ldr r1, [r0]
```

r1: 42

Step I: use ldr to put its address into a register...

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```
.data
first_int:
   .word 42
second_int:
   .word 38

.text
ldr r0, =first_int
```

Step 2: use str to write a value at that address

```
.data
first_int:
   .word 42
second_int:
   .word 38

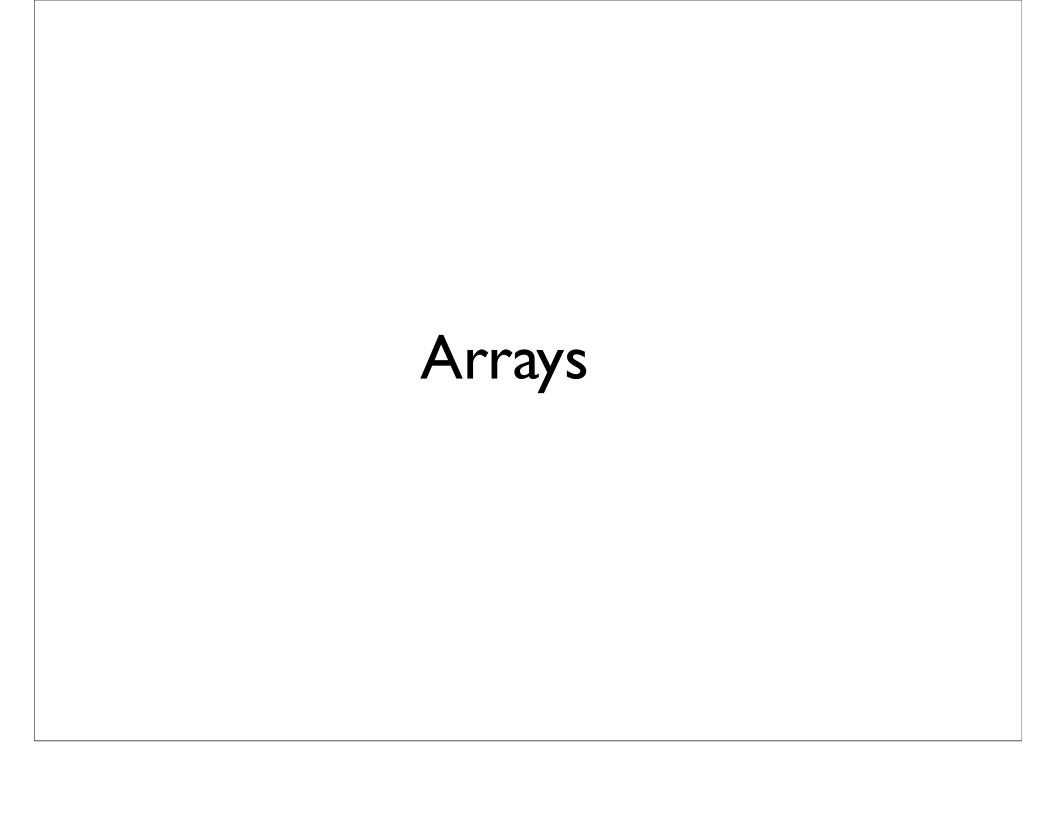
.text
ldr r0, =first_int
```

Step 2: use str to write a value at that address

```
.data
first int:
  .word 42 57
second int:
  .word 38
  .text
ldr r0, =first int
mov r1, #57
str r1, [r0]
```

## Example:

memory\_variables.s



## Specifying Arrays

Only distinction from variables: multiple values are specified with the .word directive

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Only distinction from variables: multiple values are specified with the .word directive

```
.data
first_int:
.word 42
```

## Specifying Arrays

Only distinction from variables: multiple values are specified with the .word directive

```
.data
first_int:
    .word 42
array:
    .word 32, 65, 76, 87
```

Basic approach: increment memory address

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```
.data
arr:
  .word 32, 65, 76
  .text
ldr r0, = arr
ldr r1, [r0]
add r0, r0, #4
ldr r2, [r0]
add r0, r0, #4
ldr r3, [r0]
```

<sup>-</sup>Offsets increment by 4 because one word is 4 bytes

Basic approach: increment memory address

```
.data
arr:
  .word 32, 65, 76
  .text
ldr r0, = arr
                 r1: 32
ldr r1, [r0]
add r0, r0, #4
                 r2: 65
ldr r2, [r0]
add r0, r0, #4
                 r3: 76
ldr r3, [r0]
```

Basic approach: increment memory address

.data	32	65	76
arr: .word 32, 65,		arr + 4	arr + 8
.text	1 20		
ldr r0, =arr ldr r1, [r0]	r1: 32		
add r0, r0, #4 ldr r2, [r0]	r2: 65		
add r0, r0, #4 ldr r3, [r0]	r3: 76		

<sup>-</sup>Top right corner shows memory layout in terms of arr

## Example:

register\_indirect.s

#### More on Memory Access

ldr r3, [r0]

- The above instruction uses the register indirect addressing mode
  - Addressing mode: how the processor accesses something
  - Register indirect: Memory access is done through an address in a register
- Many more available: see register \*.s

#### **ARM** addressing Modes

Name	Alternative Name	ARM Examples
Register to register	Register direct	MOV RO, R1
No. of the Control of		LDR RO, MEM
	Immediate	MOV R0, #15 ADD R1, R2, #12
Indexed, base	Register indirect	LDR R0, [R1]
Pre-indexed, base with displacement	Register indirect with offset	LDR R0, [R1, #4]
Pre-indexed, autoindexing	Register indirect pre-incrementing	LDR R0, [R1, #4]!
Post-indexing, autoindexed	Register indirect post-increment	LDR R0, [R1], #4
Double Reg indirect	Register indirect Register indexed	LDR R0, [R1, R2]
Double Reg indirect with scaling	Register indirect indexed with scaling	LDR R0, [R1, r2, LSL #2]
Program counter relative		LDR RO, [PC, #offset]

#### **ARM** addressing Modes

Addressing Mode	<b>Assembly Mnemonic</b>	Effective address	FinalValue in R1
Indexed, base Register indirect	LDR R0, [R1]	R1	R1
Pre-indexed, base with displacement	LDR R0, [R1, #d]	R1 + d	R1
Pre-indexed, autoindexing	LDR R0, [R1, #d]!	R1 + d	R1 + d
Post-indexed, autoindexed	LDR RO, [R1], #d	R1	R1 + d
Double Reg indirect	LDR R0, [R1, R2]	R1 + R2	R1
Double Reg indirect with scaling	LDR RO, [R1, R2, LSL #2]		

#### Array Access Example:

print\_array\_fixed\_length.s

## Writing to Array Example:

write array increasing.s



print\_array\_variable\_length.s